Using the KAD/DSI/002

TEC/NOT/047

The KAD/DSI/002 can monitor up to 24 differential or single ended, discrete channels. Eight of these channels (channels 0 to 7) act as special function counters, with multiple functions possible for each counter.

This paper describes how to set up the KAD/DSI/002 including details of counter settings and event tagging options. It is divided into the following sections:

23.1 Physical interface details

All 24 channels have an identical physical interface as shown in the following figure.

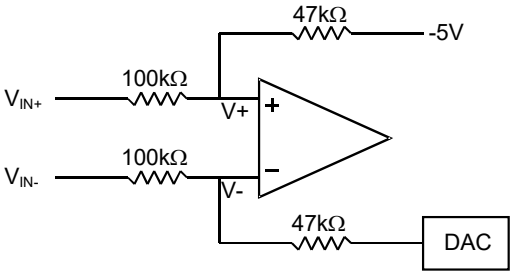

Figure 23-1: Physical interface of a channel

23.2 Setting threshold voltages

When V_+ is greater than V_-, the comparator output for each channel switches from logic 0 to logic 1. Therefore, the threshold voltage (V_T) can be defined as the point where V_+ is equal to V_-.

From the superposition theorem:

$$V_+ = \left(\frac{47}{147}\right)(V_{IN+}) + (-5)\left(\frac{100}{147}\right)$$

and

$$V_- = \left(\frac{47}{147}\right)(V_{IN-}) + (V_{DAC})\left(\frac{100}{147}\right)$$

At the threshold voltage, V_+ is equal to V_-. Therefore, the condition required for the output to switch from logic 0 to logic 1 is the following:

$$V_{IN+} - V_{IN-} > \left(\frac{100}{47}\right)(V_{DAC} + 5)$$

The above equation also expresses the relationship between the threshold voltage for each channel and the V_{DAC} (Voltage across the Digital-to-Analog Converter) as outlined in the following table.

Table 23-1: Relationship between V_{DAC} voltages and threshold voltages for the KAD/DSI/002

V_{DAC} (V)	Threshold (V_T)	V_{DAC} (V)	Threshold (V_T)
-7.350	-5.000	0.000	10.638
-7.000	-4.255	0.500	11.702
-6.500	-3.191	1.000	12.766
-6.000	-2.128	1.500	13.830
-5.500	-1.064	2.000	14.894
-5.000	0.000	2.500	15.957
-4.500	1.064	3.000	17.021
-4.000	2.128	3.500	18.085
-3.500	3.191	4.000	19.149
-3.000	4.255	4.500	20.213
-2.500	5.319	5.000	21.277
-2.000	6.383	5.500	22.340
-1.500	7.447	6.000	23.404
-1.000	8.511	6.500	24.468
-0.500	9.574	6.750	25.000

Expressed another way, V_{IN+} must be greater than V_{IN-} by the threshold voltage (V_T), which is equal to the following:

$$V_T = \left(\frac{100}{47}\right)(V_{DAC} + 5)$$

KSM-500 software (used to configure the KAD/DSI/002 module) allows you to specify the threshold, in volts, for each channel as shown in the following figure.

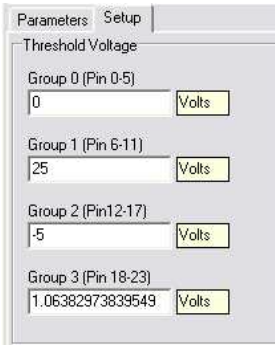

Figure 23-2: Channel threshold settings

After the threshold voltage has been specified using the software, the DAC (Digital-to-Analog Converter) is set automatically.

23.2.1 Channels per DAC

There are four DACs on a KAD/DSI/002, spread between the 24 input channels. Each DAC controls the threshold voltage for a group of six channels as shown in the following table.

Table 23-2: Channels per DAC

DAC	Channels
DAC1	Channels 0 to 7.
DAC2	Channels 8 to 15.
DAC3	Channels 16 to 23.
DAC4	Channels 24 to 31.

23.2.2 Examples of threshold settings

The following examples outline suitable threshold settings which correspond to various electrical inputs for the KAD/DSI/002. Recommended electrical inputs for particular threshold settings are also covered.

23.2.2.1 When both inputs are connected to defined voltages

When V_{IN+} and V_{IN-} are switched between known voltages, that is, never left floating, each input behaves according to the following principle:

V_{IN+} must be greater than V_{IN-} by an amount greater than, or equal to, the threshold voltage in order to read a logic 1 for that channel.

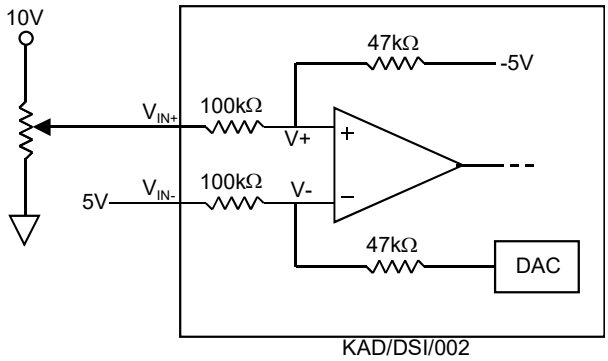

Figure 23-3: Threshold settings when both inputs are connected to defined voltages

Therefore, when a KAD/DSI/002 channel is connected as shown in the previous figure, the comparator outputs logic 0 when:

$$V_{IN+} \leq 5V + V_T$$

The comparator outputs a logic 1 when:

$$V_{IN+} > 5V + V_T$$

Therefore, if the threshold voltage is set to 0V, the comparator output switches from logic 0 to logic 1 when the input voltage (V_{IN+}) is greater than 5V.

Also, should the threshold voltage be set to, say 4V, the comparator output switches from logic 0 to logic 1 when the input voltage (V_{IN+}) is greater than 9V.

23.2.2.2 When setting a channel for 0V/Open

You can set the KAD/DSI/002 input channel to read a 0V/Open discrete signal (see the following figure).

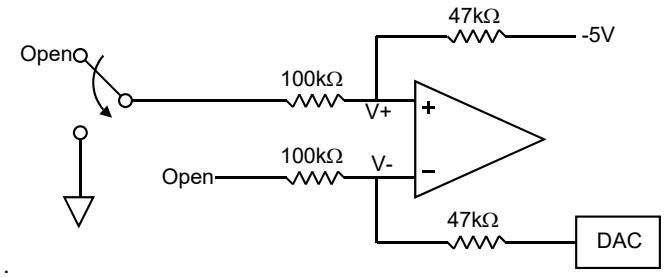

Figure 23-4: Threshold settings for 0V/Open

To set up a channel for 0V/Open, leave the negative input pin floating. This ensures that V_- floats to whatever the V_{DAC} is set to. When the switch is in the Open position, V_+ and V_{IN+} float to -5V. When the switch is in the 0V position, V_+ increases to approximately -3.4V due to the voltage divider at the input (see the following figure).

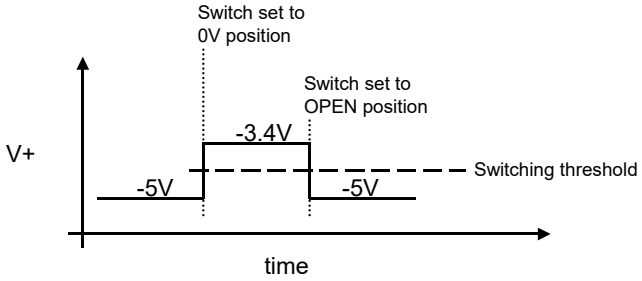

Figure 23-5: Position of switches relative to switching threshold voltage

You should set the V_{DAC} to a value between -3.4V and -5V (typically, in the middle of this range—approximately -4.2V). According to Table 23-1 on page 2, the threshold should be set to approximately 1.7V.

The group of six channels which the channel belongs to should be set with a threshold of 1.7V. To achieve this, the software automatically sets the DAC to the appropriate voltage (in this case, -4.2V). If you are setting up the module through the XID, XML or XidML files, you can set the DAC voltage directly in the syntax.

23.2.2.3 When setting a channel for 28V/Open

You can set the KAD/DSI/002 input channel to read a 28V/Open discrete signal (see the following figure).

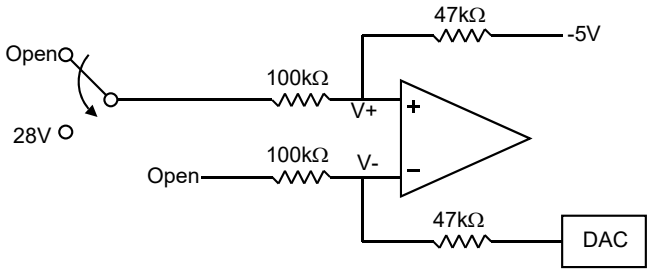

Figure 23-6: Threshold settings for 28V/Open

To set up a channel for 28V/Open, leave the negative input pin floating. This ensures that V_- floats to whatever V_{DAC} is set to. When the switch is in the Open position, V_+ floats to -5V. When the switch is in the 28V position, V_+ increases to approximately 5.55V due to the voltage divider at the input.

Therefore, the DAC voltage should be set to a value between -5V and 5.55V. Typically, you could choose somewhere in the middle of this range, that is, 0V. According to Table 23-1 on page 2, the threshold value in the software is to be set to approximately 10V.

23.2.2.4 When setting a channel for 28V/0V

You can set the KAD/DSI/002 input channel to read a 28V/0V discrete signal (see the following figure).

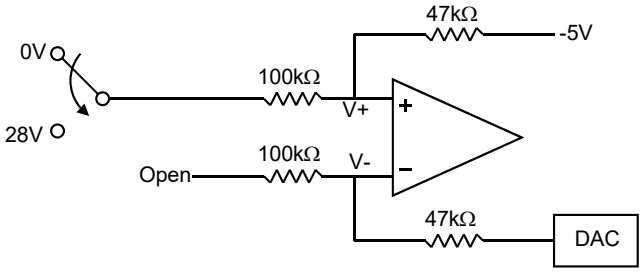

Figure 23-7: Threshold settings for 28V/0V

To set up a channel for 28V/OV, leave the negative input pin floating. This ensures that V- floats to whatever V_{DAC} is set to. When the switch is in the 0V position, V_+ is approximately -3.4V. When the switch is in the 28V position, V_+ increases to approximately +5.55V.

Therefore, the DAC voltage should be set to a value between -3.4V and +5.55V. Typically, you could select somewhere in the middle of this range, that is, +1V. According to Table 23-1 on page 2, the threshold value in the software is to be set to approximately 12V.

23.2.2.5 Other options

All examples given here involve the floating of the negative input. However, it is possible to leave the positive input floating (in which case V_+ always floats to -5V) and connect the negative input to the discrete signal (such as 0V/Open or 28V/0V).

When left unconnected, the negative input pin floats to the DAC output voltage, which can be set between -7.35V and 6.75V, with 3.663 mV steps. That is, 12-bit DAC in the range ±7.5V; however not all of the range is usable.

23.3 Special function registers

The first eight channels of the KAD/DSI/002 are connected to special function registers, which you can configure on a channel-by-channel basis to read the following:

- The number of clock cycles between events on a channel
- The number of events on a channel in a defined clock period
- The number of events since the register was previously read
- The time elapsed since the register was previously read
- The number of events updated on a sample since power-up
- The total number of clocks on the channel
- Each time the register is read
- The total number of events on a channel

The following figure shows how these registers can be set in the software.

Parameters | Setup

Parameter Name	Mode	Type	Output	Edge	Clock	Protocols	Comment
DSI2_0_J7_CTR0	COUNTER_0	PERIOD	BCD	Rising	1s	None	
DSI2_0_J7_CTR1	COUNTER_1	FREQUENCY	BIN	Falling	1ms	None	
DSI2_0_J7_CTR2	COUNTER_2	EVENT_SINCE	BCD	Rising	N/A	None	
DSI2_0_J7_CTR3	COUNTER_3	ELAPSED	BIN	Falling	125ns	None	
DSI2_0_J7_CTR4	COUNTER_4	COUNT	BCD	Rising	125ns	None	
DSI2_0_J7_CTR5	COUNTER_5	TIMER	BIN	Falling	125ns	None	
DSI2_0_J7_CTR6	COUNTER_6	READ	BCD	N/A	N/A	None	
DSI2_0_J7_CTR7	COUNTER_7	EVENT	BIN	Rising	N/A	None	
DSI2_STAT_HI_0_J7	STATUS[23-12]	N/A	N/A	N/A	N/A	None	
DSI2_STAT_LO_0_J7	STATUS[11-0]	N/A	N/A	N/A	N/A	None	
DSI2_TAG_EV_0_J7	TAG_EVENT	N/A	N/A	N/A	N/A	None	

Figure 23-8: Register settings in kSetup

You can set the output of each special function register to display in BINary (BIN) or Binary Coded Decimal (BCD). You can also configure each special function register to count on either rising or falling edges of a signal.

23.3.1 PERIOD

This register type counts the number of clock cycles between events on a channel. To gain optimum resolution for the period measurement, select the clock frequency for the register.

To measure a signal which typically has a period of two seconds, configure the channel to measure PERIOD, with a clock time of one millisecond (ms), that is, the frequency is equal to 1 kHz. Therefore, whenever you read the special function register, expect to read a PERIOD value of 2000 (meaning that 2000 × one-millisecond clock is equal to a two-second period).

Set the period measurement clock to any value between 125 nanoseconds (ns) and one second. The register counts from 0 to 65535 (or to 9999 for BCD mode), and stays there when the maximal value has been reached.

23.3.2 FREQUENCY

This register type counts the number of events on a channel, in a defined clock period. To gain optimum resolution for the frequency measurement, select the clock frequency for the register. To measure a signal which has a frequency varying between 500 Hz and 2.5 kHz, configure the channel to measure frequency, with a clock time of one second, that is, frequency is equal to 1 Hz.

Therefore, whenever you read the FREQUENCY register, expect to read a period value of somewhere between 500 and 2500 events, since that is the number of events on that channel between one-second clock periods.

Similarly, should you set the clock frequency on the channel to be 10 Hz, that is, the clock period is equal to 100 ms, then expect to read values between 50 and 250 events whenever you read the FREQUENCY register.

You can set the frequency measurement clock to any value between 125 ns and one second. Setting the clock period to one second means that any frequency result is in Hertz. The register counts from 0 to 65535 and stays at 65535 when the maximal value has been reached.

23.3.3 EVENT_SINCE

This register type counts the number of events since the register was previously read. Thus, events on the channel increment the counter, and the counter is cleared each time it is read. The register counts from 0 to 65535 and stays at 65535 when the maximal value has been reached.

23.3.4 ELAPSED

This register type counts the time elapsed since the register was previously read. Clock pulses on the channel increment the counter, and the counter is cleared each time it is read. The register counts from 0 to 65535 (or to 9999 for BCD mode), and stays there when the maximal value has been reached.

23.3.5 COUNT

This register type counts the number of events since power-up. The register counts from 0 to 65535 (or to 9999 for BCD mode), incrementing each time an event updates on a sample, and rolls back to 0 after the maximal value has been reached.

23.3.6 TIMER

This counter increments using a pre-selected clock. In this mode, the register counts the total number of clocks on the channel since the last event. As per period measurement, the clock period may be set at any value between 125 ns and one second. The register counts from 0 to 65535 (or to 9999 for BCD mode), and stays there when the maximal value has been reached.

23.3.7 READ

This register type counts each time the register is read. The register counts from 0 to 65535 (or to 9999 for BCD mode), incrementing each time it is read, and rolls over to 1 after the maximal value has been reached.

23.3.8 EVENT

This register type counts the total number of samples since the last event on a channel. The register increments when every sample is read on the channel counting up to 65535 (or to 9999 for BCD mode), and resets to 1 on a new event.

23.3.9 STATUS

All 24 channels may be sampled to give a snapshot of whether they are logic 1 or logic 0 at any time. The status of the 24 channels is available to read typically as 2 × 12-bit STATUS words, with 12 of the status values in each of the 12-bit words.

23.4 Event tagging

You can configure the last 16 channels as event tagging channels. The range of each counter is programmable as is voltage threshold and sensitivity to the rising and falling edge. Events are triggered when the channel has either a rising or falling edge. You can use the last 16 of the 24 channels for event tagging.

Event tagging means that every time an event occurs on a channel, a 48-bit word is generated for that event. This 48-bit word contains the following information:

- Status of Channels 7 to 23 inclusive (16 bits)
- Lo Time (16 bits)
- Micro Time (16 bits)

Lo Time and Micro Time are the time stamps for when the event happened.

48-bit event tag words are stored in an event buffer which is 1K deep. This buffer must be read frequently so that it does not overflow.

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